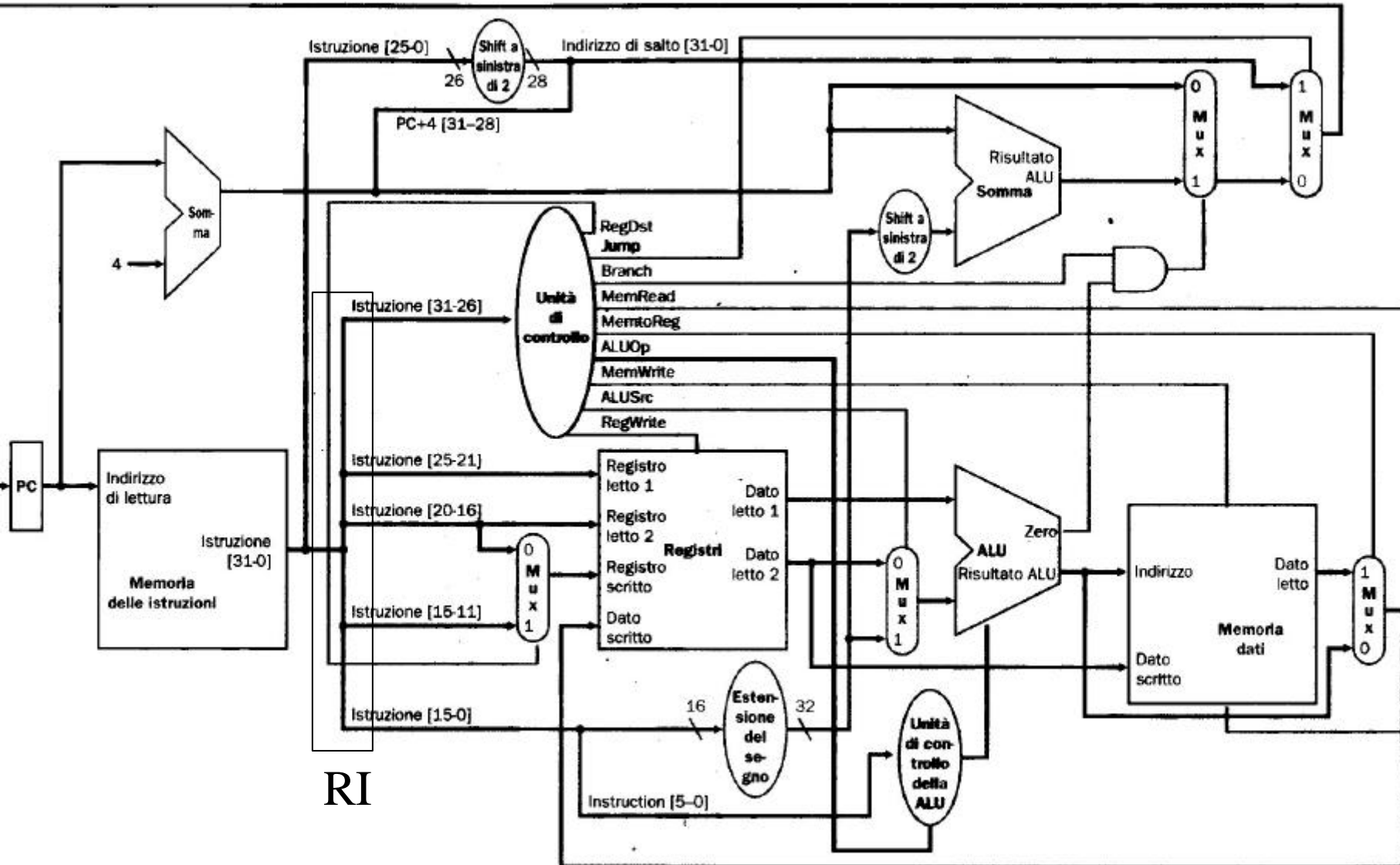
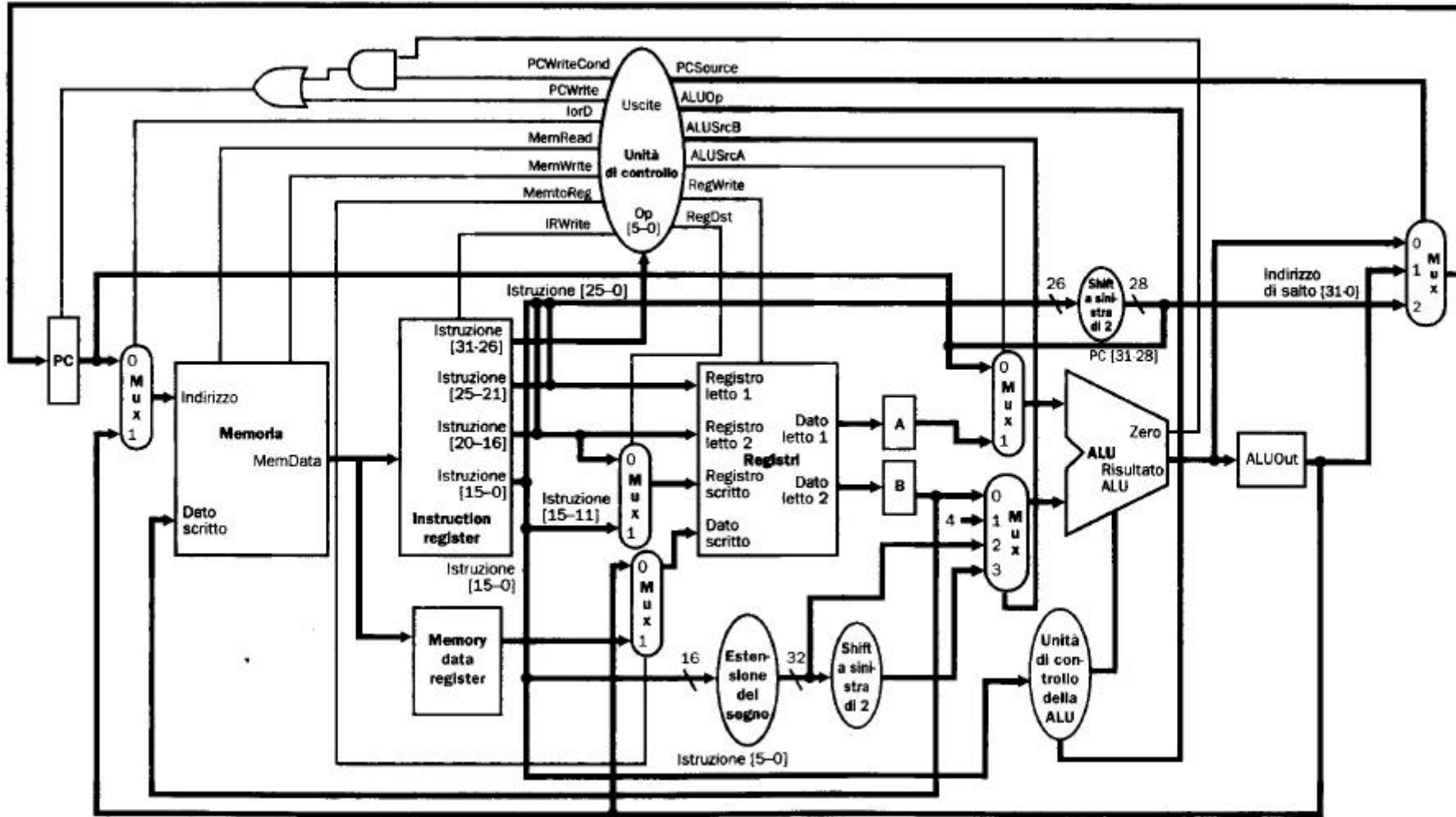


# **Schemi circuitali analizzati nel corso di architetture I**

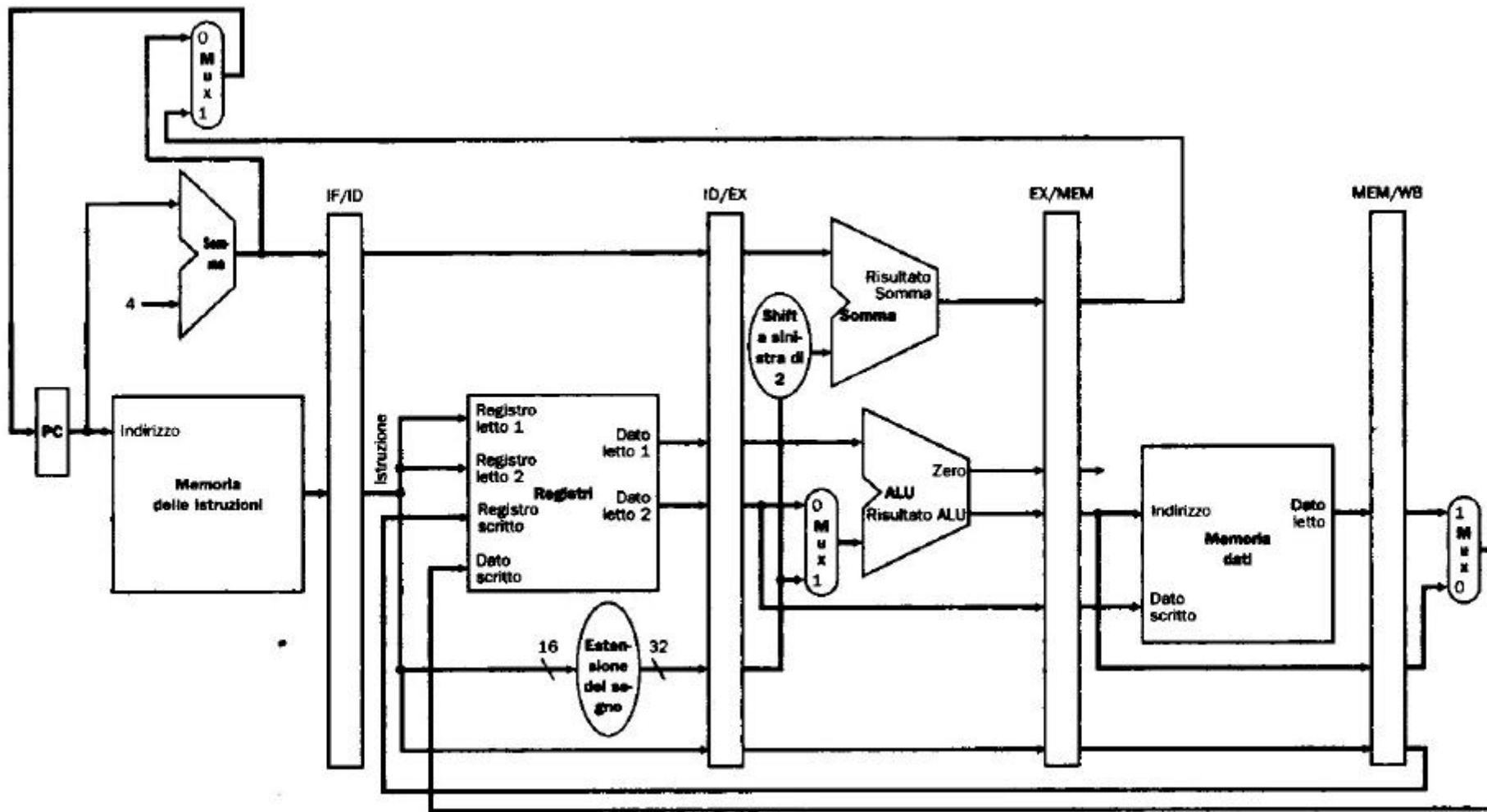
# CPU a singolo ciclo



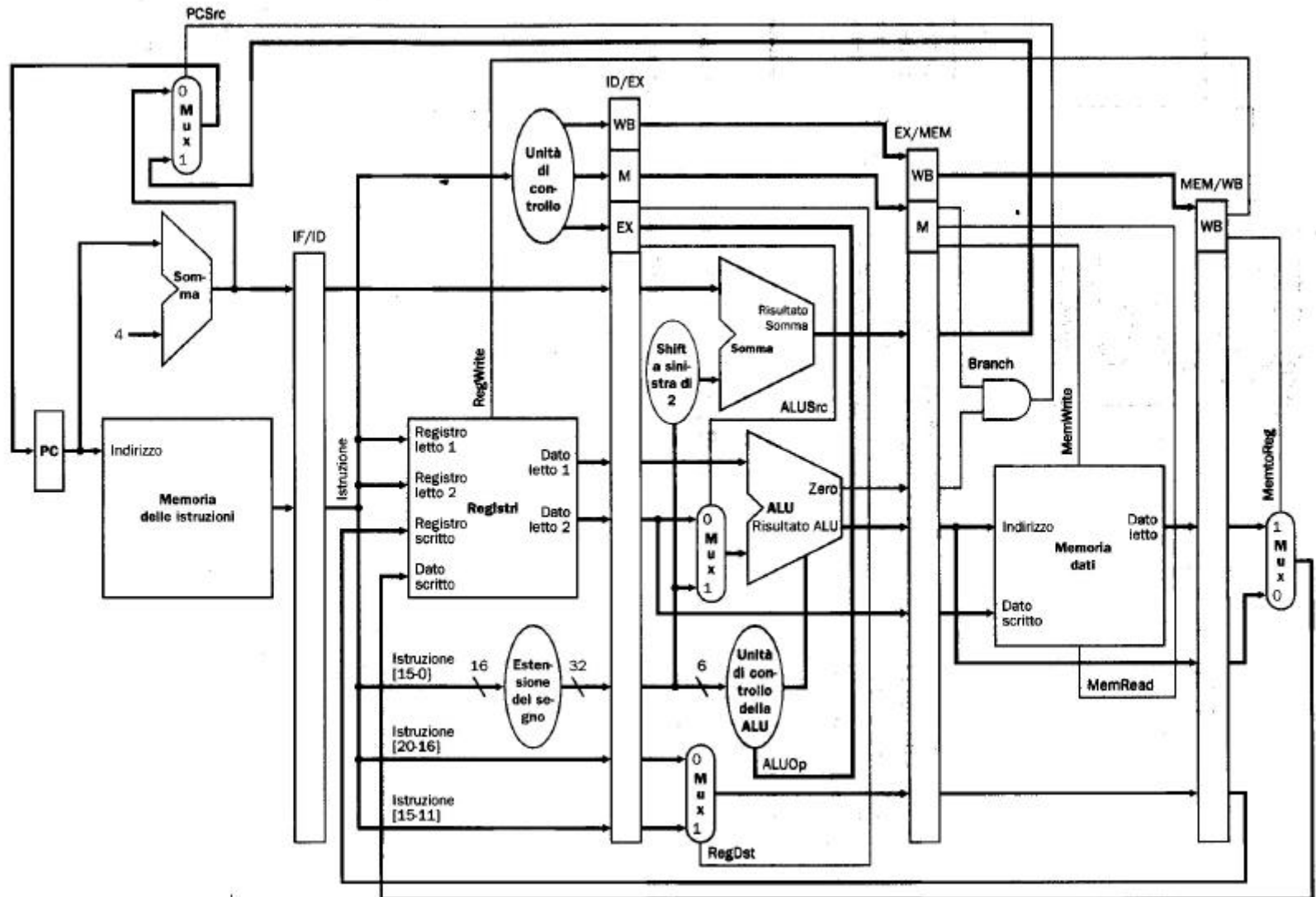
# CPU multi-ciclo



# CPU con Pipeline



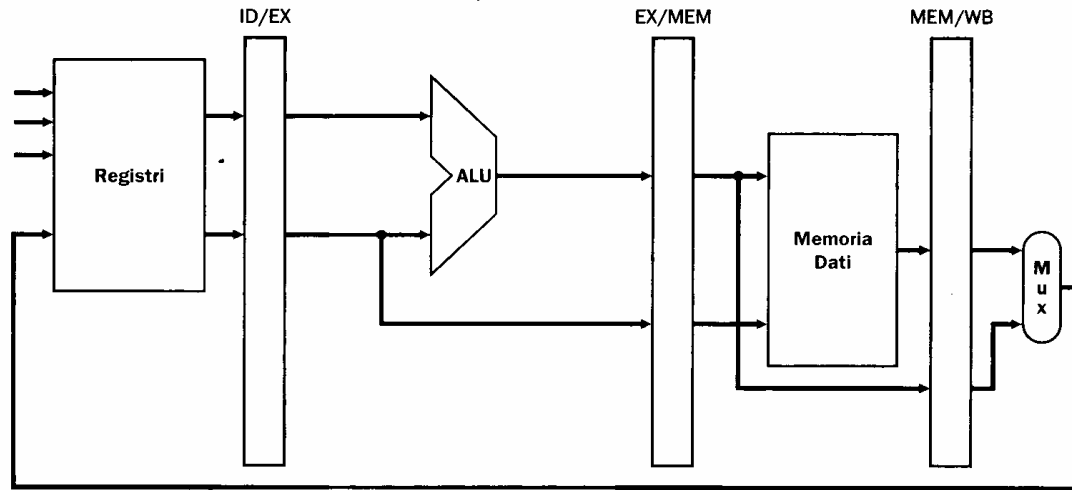
# CPU con pipeline



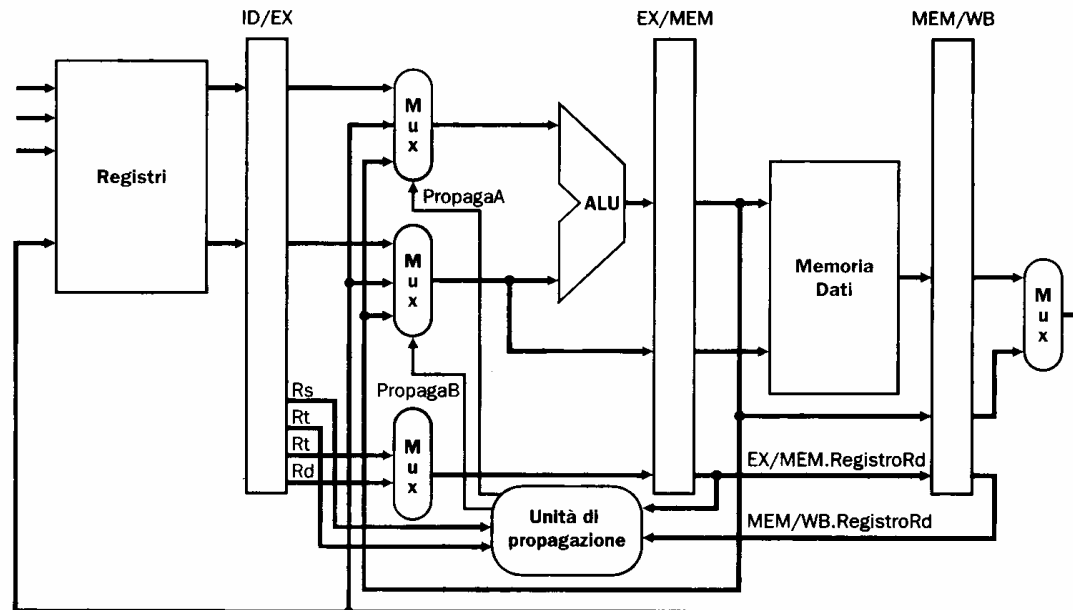
# Unità funzionali della pipeline



# Gestione degli hazard aritmetici



a. Senza propagazione







# CPU con pipe-line + hazard

