


Circuiti Digitali

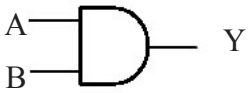

NOT

A	Y
0	1
1	0

"Inverter logico"

Porta AND

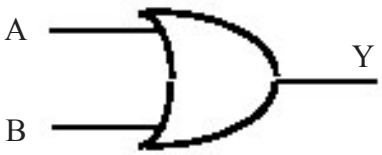
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



"Prodotto logico"

Porta OR

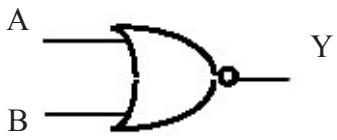
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



"Somma logica"

Porta NOR

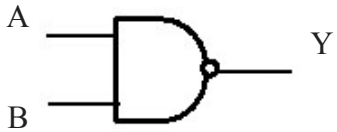
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



"Not(Or(A,B))"

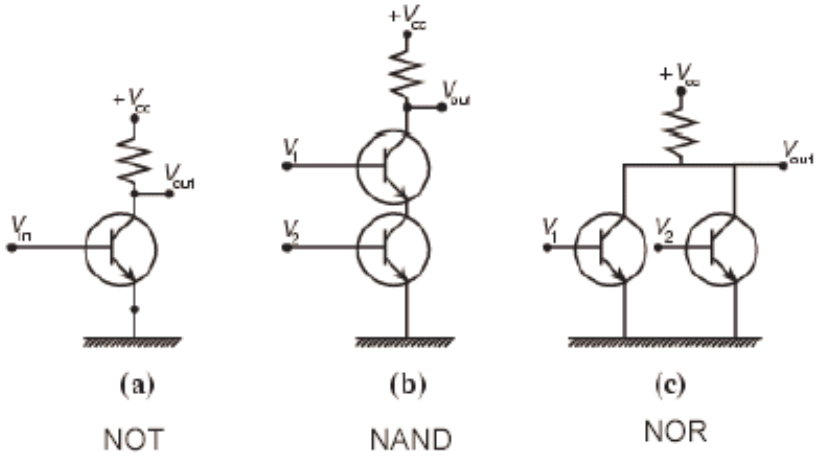
Porta NAND

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

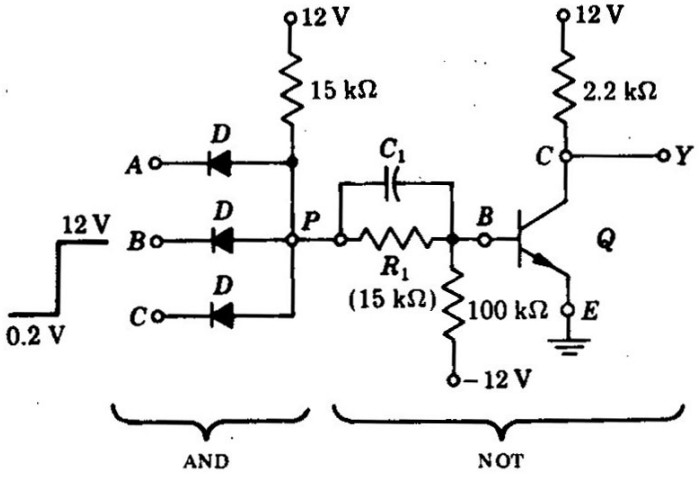


"Not(And(A,B))"

Circuiti di base

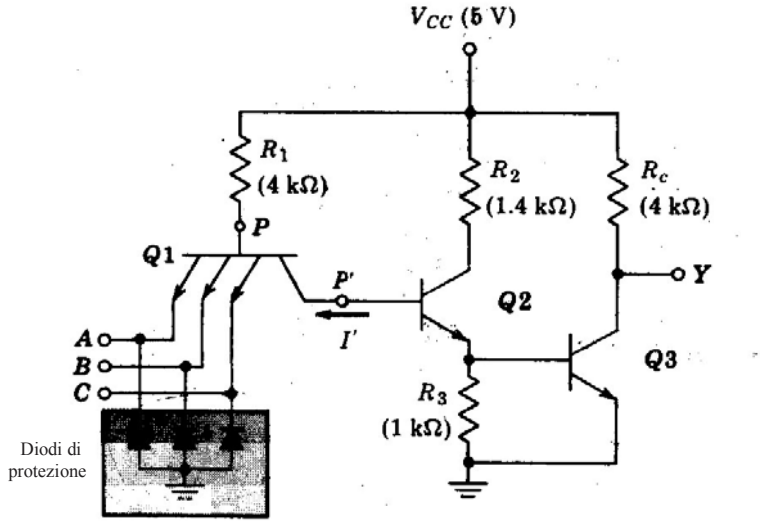


Logica RTL



Porta NAND a 3 ingressi in Resistor Transistor Logic (RTL).

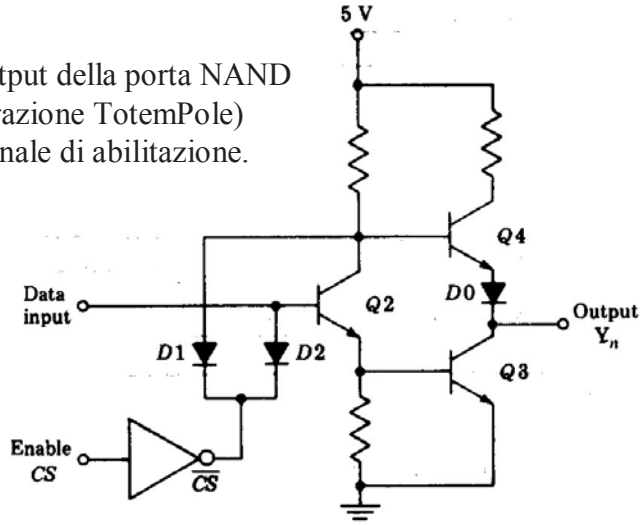
Logica TTL



Porta NAND in Transitor-Transistor-Logic.

Logica TTL three-state

Stadio di output della porta NAND (configurazione TotemPole) con il segnale di abilitazione.



CS = 0 → Chip enabled

Logica TTL three-state

Stadio di output della porta NAND
(configurazione TotemPole)
con il segnale di abilitazione.