



Architetture degli Elaboratori e delle Reti I

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Laboratorio - linea 3 (M-Z)

CPU



Simulazione CPU – 1

(componenti fondamentali)

Register File

ALU

Memoria

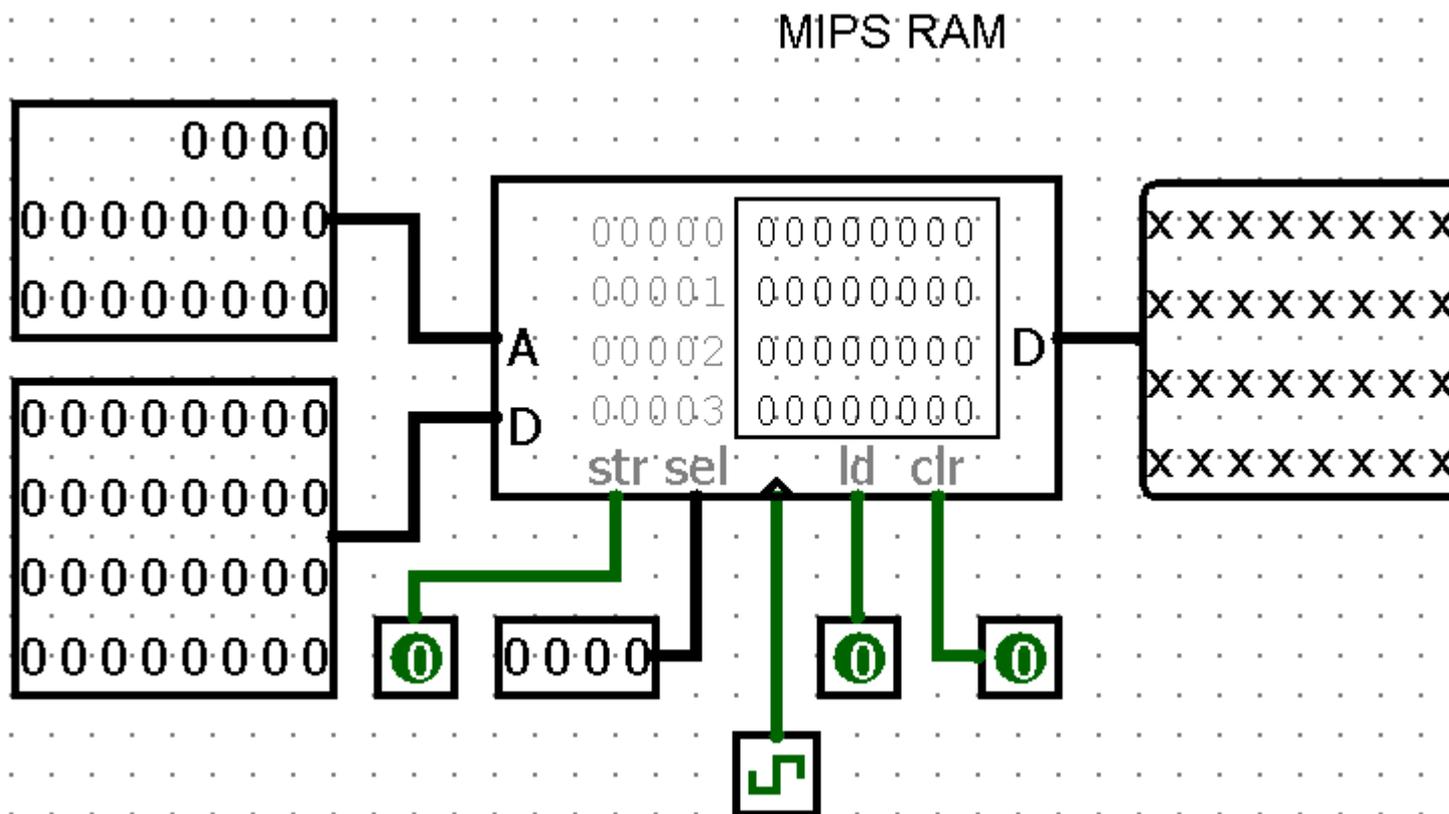


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Memoria





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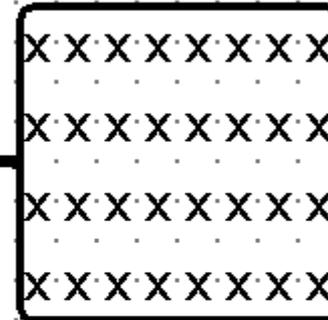
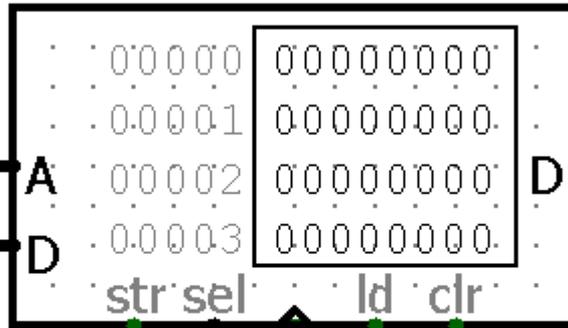
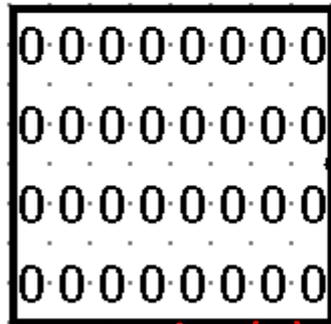
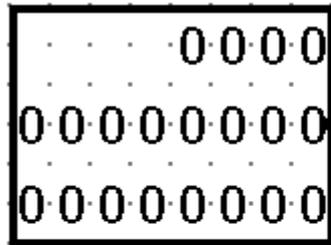
10

Laboratorio - linea 2 (M-Z)

Memoria

MIPS RAM

Address selector (A)



Input value (D)

bytes mask
(access
enable if 1)

Asynchronous reset

Write input at
selected address

Read value at selected
address



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Laboratorio - linea 3 (M-Z)

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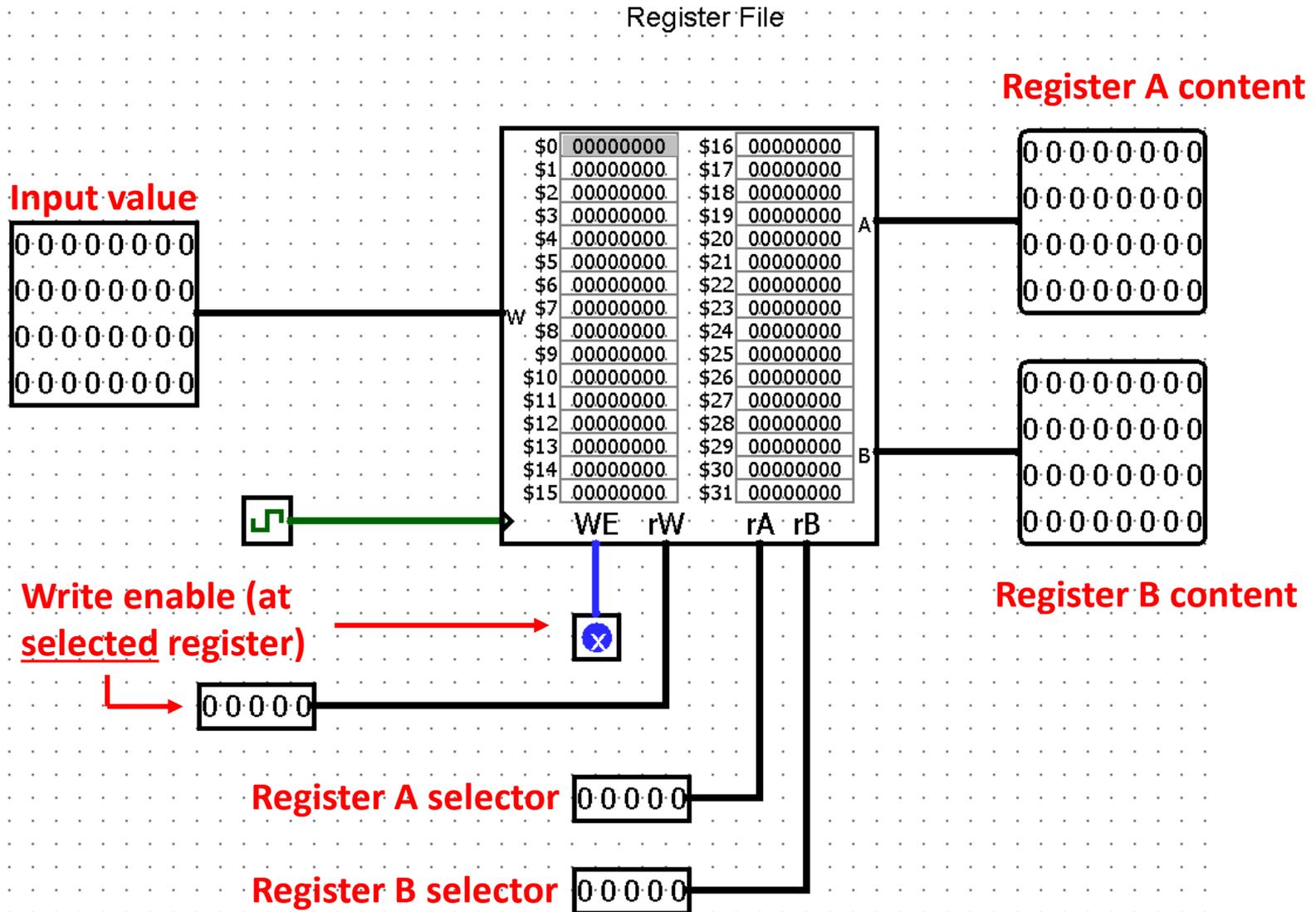
Register File



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Laboratorio - linea 3 (M-Z)



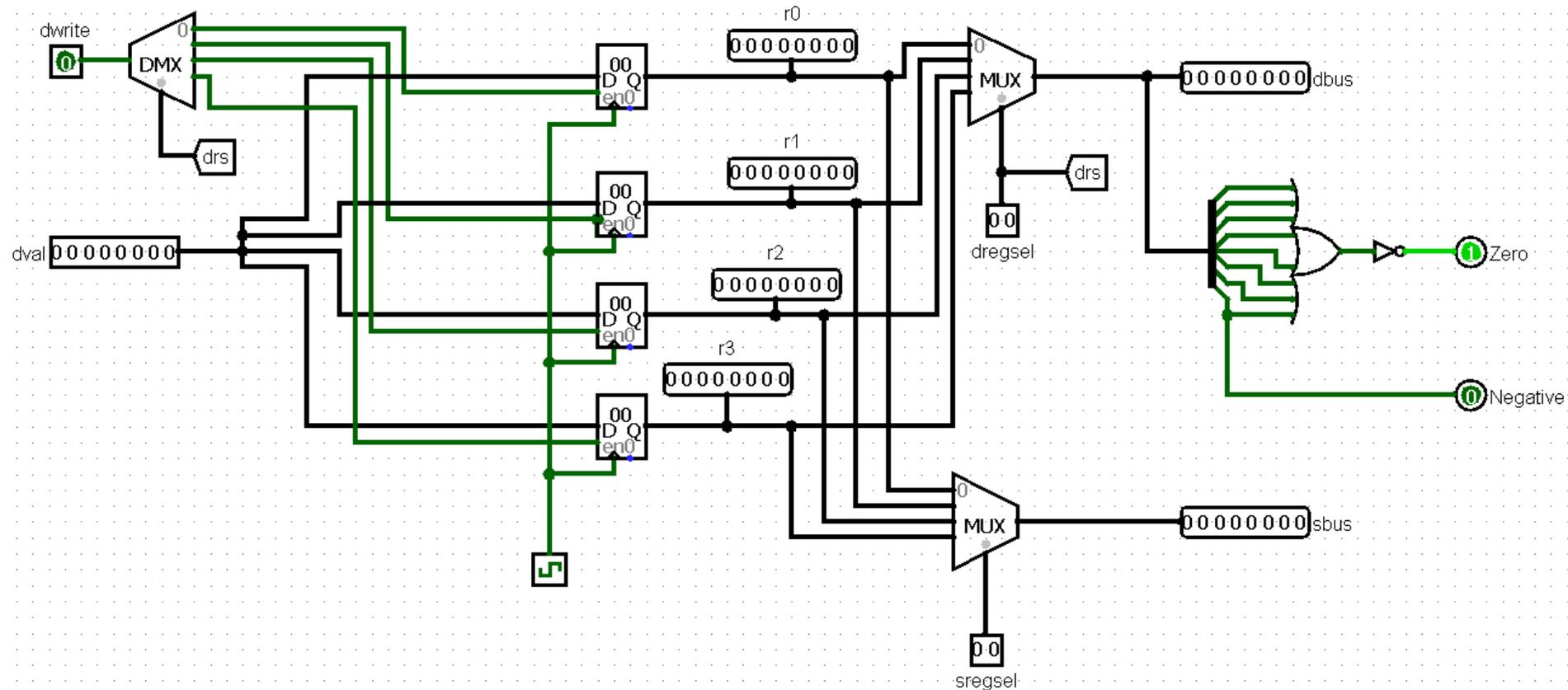


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Laboratorio - linea 3 (M-Z)

Register File



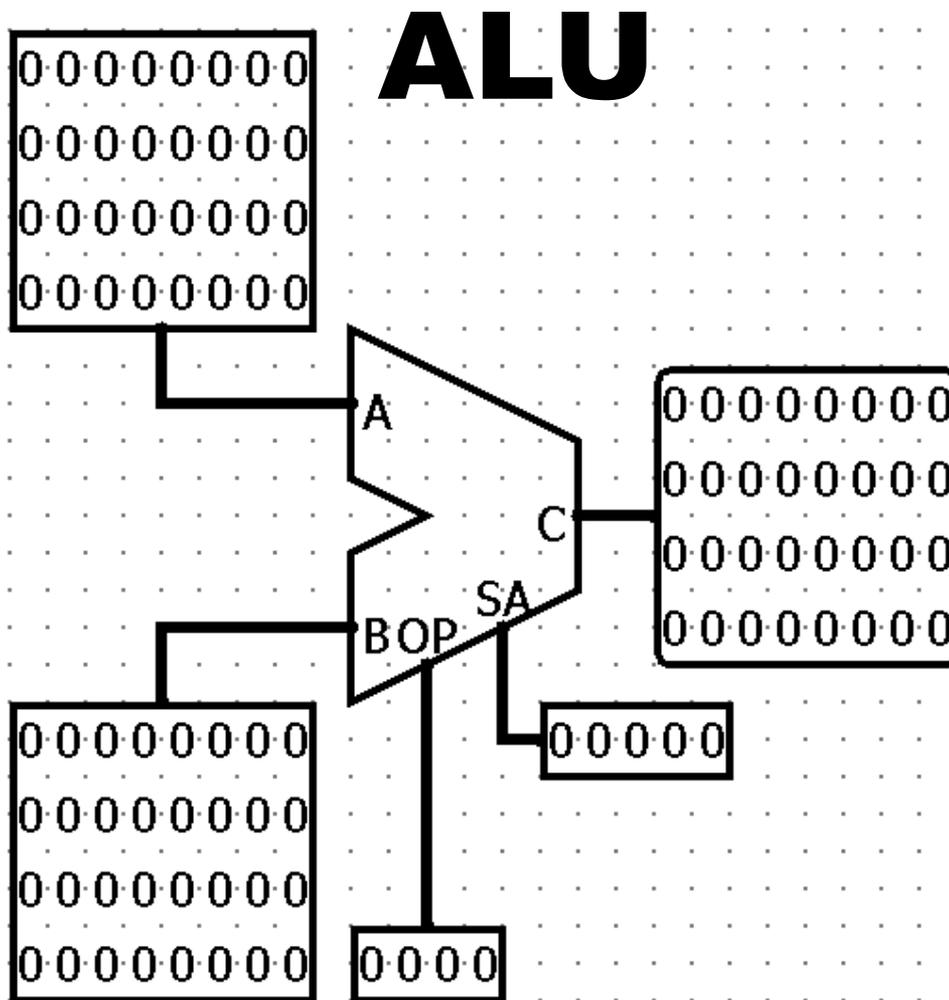
Implementazione mediante componenti libreria standard Logisim



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Laboratorio - linea 3 (M-Z)



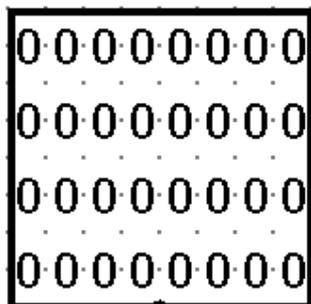


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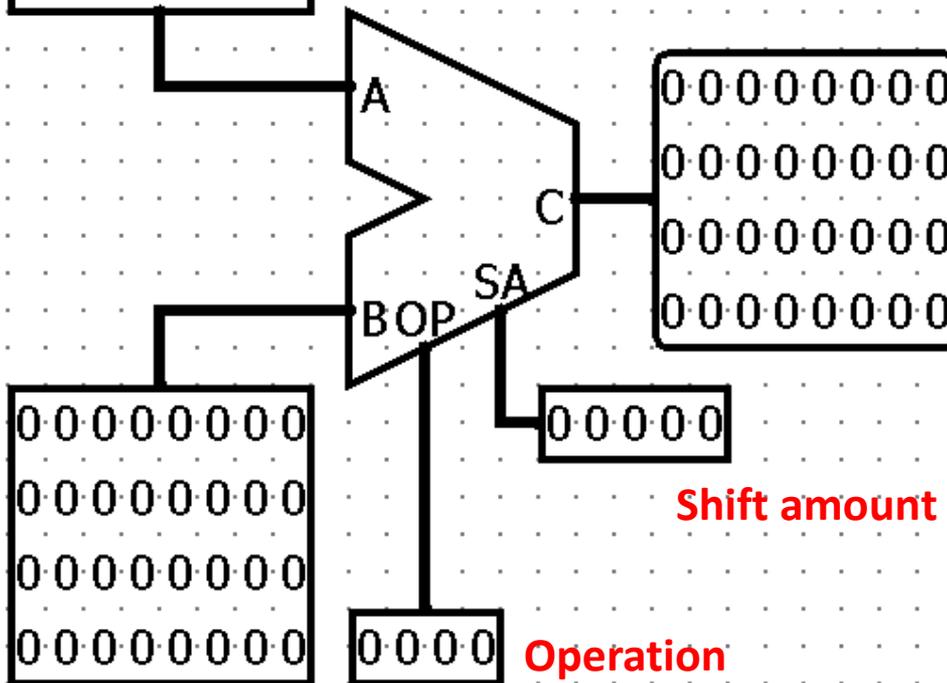
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Laboratorio - linea 3 (M-Z)

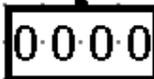
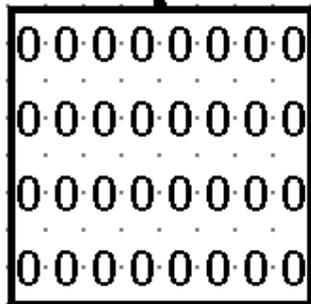
Input value A



ALU

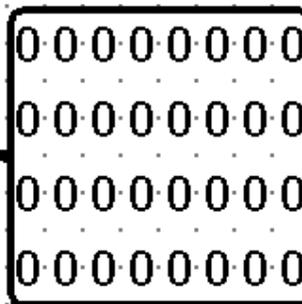


Input value B

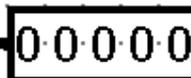


Operation

Output value C



Shift amount





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MIPS ALU. Computes a result as follows:

Op	name	C
000x	shift left	$C = B \ll S_a;$
001x	add	$C = A + B$
0100	shift right logical	$C = B \ggg S_a$
0101	shift right arithmetic	$C = B \gg S_a$
011x	subtract	$C = A - B$
1000	and	$C = A \& B$
1010	or	$C = A B$
1100	xor	$C = A \wedge B$
1110	nor	$C = \sim(A B)$
1001	eq	$C = (A == B) ? 1 : 0$
1011	ne	$C = (A != B) ? 1 : 0$
1101	gtz	$C = (A > 0) ? 1 : 0$
1111	lez	$C = (A \leq 0) ? 1 : 0$