Short Curriculum Vitae

Valentina Ciriani
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Personal Details

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Career and Education

Academic Positions

[2015–] Associate Professor, Department of Computer Science, University of Milano, Italy.
[2005–2015] Assistant Professor, Department of Computer Science, University of Milano, Italy.
[2003–2005] Research Fellow, Department of Computer Science, University of Pisa, Italy.

National Scientific Qualification (Abilitazioni)

[2014] National Scientific Qualification (abilitazione) as Associate Professor in Computer Science.
[2020] National Scientific Qualification (abilitazione) as Full Professor in Computer Science.

Education

[2002] Ph.D., Computer Science,Thesis: "Three-Level Logic Synthesis: Algebraic Approach and Minimization Algorithms", Advisor: Prof. Fabrizio Luccio, University of Pisa, Italy.
[1998] M.A. (*Laurea* degree, Summa cum Laude), Computer Science, University of Pisa, Italy.

Research and Scientific Publications

Research Interests

The main research interests are, in general, design automation of integrated circuits, logic synthesis, and security. In particular:

- algorithms and data structures for *synthesis of logic circuits* and networks;
- circuit optimization for *emerging technologies*;
- *hardware minimization for security* protocols.

Considering DAC research categories, the research interests are:

EDA4. RTL/Logic Level and High-level Synthesis, in particular:

EDA4.1 Combinational, sequential and asynchronous logic synthesis
EDA4.5 Synthesis for circuits in emerging device technologies

DES3. Emerging Models of Computation

DES5. Emerging Device Technologies, in particular:

DES5.2 Nanotechnologies, nanowires, nanotubes

SEC1. Hardware Security, in particular:

SEC1.1 Hardware security primitives

Short Description of the Research Activity

- *Logic Synthesis and Optimization*: The research activity is focused on the design and implementation of efficient synthesis algorithms to synthesize compact circuits with a constant number of levels (and therefore a bounded delay). Theoretical studies and experimental results have shown that these circuits have a compact area, a constant delay and can be minimized in reasonable computational times. Moreover, the proposed synthesis algorithms guarantee good circuits properties such as testability and low power consumption. The main contribution in this area is the formal study of new compact multilevel logic networks and the innovative approach to logic minimization via affine spaces, the exploitation of regular properties of regular properties of Boolean functions for their logic synthesis, and the use of don't care conditions for efficient decompositions into new multilevel networks with low power consumption properties.
- *Emerging Nano-Technologies*: Recently, the research is focused on the logic synthesis for emerging technologies. In particular, the main goal is developing a complete synthesis and optimization methodology for switching nano-crossbar arrays that leads to the design and construction of an emerging nanocomputer. The proposed methodology targets some emerging technologies including nanowire/nanotube crossbar arrays, magnetic switch-based structures, and crossbar memories. The results of the current research on this topic are the foundation of nano-crossbar based circuit design techniques.
- *Circuit Synthesis for Security Problems*: The research activity is mainly focused on multiparty secure computation protocols, which have been introduced to give to two parties the capability to compute a function of their inputs, while keeping their inputs private, and sharing only the final result. Yao's solution is based on the design of a Garbled Circuit (GC), which is a standard Boolean circuit representing the function to be computed securely. In this context, the main research contributions are: quantum-based approaches to reduce the number of non-XOR gates and the modeling of the problem by means of multiple-valued circuits.

Scientific Publications

The research activity has produced more than 90 publications, in particular:

- 27 publications in *international refereed journals*. Among them: 4 papers in IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems (TCAD), 2 papers in IEEE Transactions on Computers (TC), 3 papers in ACM Transactions on Design Automation of Electronic Systems (TODAES), 3 papers in Theory of Computing Systems, 1 paper in ACM Transactions on Algorithms, 1 paper in ACM Transactions on Information and System Security (TISSEC), and 2 papers in Journal of Computer Security.
- 10 publications in *international book chapters*.
- 59 publications in *refereed international conference proceedings*. Among them: 6 papers in the proceedings of Design, Automation, and Test in Europe (DATE), 2 papers in the proceedings of Design Automation Conference (DAC), 2 papers in the proceedings of ACM Great Lakes Symposium on VLSI, 1 paper in the proceedings of Annual Symposium on Foundations of Computer Science (FOCS), 1 paper in the proceedings of IEEE International Conference on Distributed Computing Systems.

Recent Invited Talks

[2015] EPFL Workshop on Logic Synthesis & Verification (organization by Giovanni De Micheli), "Logic Synthesis via Boolean Relations".

[2019] DATE 2019 Friday Workshop: Quo Vadis, Logic Synthesis?, "XOR Gates in Emerging Technologies".

Recent Research Projects

[2015–2019] *Principal Investigator for University of Milan*: European Community H2020-MSCA-RISE-2015: "NANOxCOMP: Synthesis and Performance Optimization of a Switching Nano-crossbar Computer". Total funding EUR 724,500 (about $857,000).

[2014–2017] Participant: Italian PRIN research project "AMANDA: Algorithmics for MAssive and Networked DAta". Total funding EUR 334,276 (about $395,000).

Coordination of Research Groups

From 2009 to 2015, Valentina Ciriani is responsible and coordinator of the ALOS Lab (Algorithms and Logic Synthesis) at the Computer Science Department, Milano, Italy. The main research topics at ALOS Lab are models, algorithms and data structures for the efficient synthesis of compact and testable logic circuits with low delay and low power consumption in classical and emerging technologies. From 2015 she is co-responsible of the FALSE Lab (Formal methods and Algorithms for Large-Scale systEms) at the Computer Science Department, Milano, Italy.

Principal Scientific Collaborations

- Lorena Anghel, Grenoble INP, University Grenoble-Alpes, Grenoble, France.
- Anna Bernasconi, Department of Computer Science, University of Pisa, Italy.
- Rolf Drechsler, Institute of Computer Science, University of Bremen, Germany.
- Fabrizio Luccio, Department of Computer Science, University of Pisa, Italy.
- Tiziano Villa, Department of Computer Science, University of Verona, Italy.

Conference and Journal Service

Associate Editor

- Associate Editor (Editorial Board Member) for the Elsevier journal "Microprocessors and Microsystems - Embedded Hardware Design". ISSN: 0141-933.

Organization of Scientific Conferences

[2014] Program co-chair for topic "Logic Synthesis and Timing Analysis" in *Design, Automation and Test in Europe DATE 2014*.

[2014] Program co-chair for the Special Section "Emerging technologies and circuit synthesis (ETCS)" in *Euromicro Conference on Digital System Design DSD*.

[2015] Program co-chair for the Special Section "Emerging technologies and circuit synthesis (ETCS)" in *Euromicro Conference on Digital System Design DSD*.

[2005–2018] Organization and coordination (Program Chair) of the "National Days of Logic Synthesis": Italian workshop on the latest research developments in Logic Synthesis.

PC Member

[2010–2016] *Design, Automation and Test in Europe (DATE)*.

[2020] *Design Automation Conference (DAC)* (Late Breaking Results).

[2009] *Euromicro Conference on Digital System Design (DSD)* (Special Session "Logic Synthesis Hot Anew").

[2018–2020] *Euromicro Conference on Digital System Design (DSD)* (Special Session "Future Trends in Emerging Technologies").

[2008, 2010] *Workshop on Privacy and Security by means of Artificial Intelligence*.

[2009–2011] *Workshop on Data Privacy Management (DPM).*

[2011] *Workshop on Model-Based and Policy-Based Engineering in Information Security (MPEIS).*

[2018, 2020] *International Workshop on Boolean Problems (IWSBP).*

[2018–2020] *International Conference on Microelectronic Devices and Technologies (MicDAT).*

[2019] *Reed-Muller Workshop (RM).*

[2020–2021] *International Conference on Electrical Engineering and Electronics (EEE)*

[2020] *Design Automation Conference (DAC), Late Breaking Results*

Reviewer for International Journals

Valentina Ciriani has been reviewer for many international journals, among them: IEEE TCAD, IEEE TC, Proceeding IEEE, IEEE TVLSI, ACM TALG, ACM TKDD, and ACM TODS.